DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mark Marcelli on 7/3/08.

The application has been amended as follows:

Claims 1 - 10. (Cancelled)

11. (Currently Amended): An SOI device having a gate, comprising:

oxygen ions providing discrete implant regions in a substrate of an SOI device, the discrete implant regions extending to a surface of the substrate;

one or more additional gate regions forming an H-gate or a T-gate and covering all discrete implant regions under the one or more additional gate regions, and

a gate oxide layer covering but not encroaching the discrete implant regions and being under the one or more additional gate regions, the gate oxide layer including a thin gate oxide layer, and a thicker gate oxide layer covering the discrete implant regions,

the discrete implant regions forming gate oxide regions and reducing substrate resistance under each of the additional gate regions.

12. (Original): The SOI device as recited in claim 11, further comprising:

implanted ions in the substrate, the one or more additional gate regions covering the implanted ions.

13. (Cancelled)

14. (Previously Presented): The SOI device as recited in claim 11, further comprising:

a gate of the SOI device.

15. (Previously Presented): The SOI device as recited in claim 11, further comprising:

a gate electrode layer forming an SOI device gate and the one or more additional gate regions.

16. (Previously Presented): The SOI device as recited in claim 11, further comprising:

an SOI device gate and the one or more additional gate regions being formed from a gate electrode layer; and

wherein the gate oxide layer is under the gate and under the one or more additional gate regions.

17. (Currently Amended): The SOI device as recited in claim 11, further comprising:

~~the gate oxide layer including a thin gate oxide layer, and a thicker gate oxide layer covering the discrete implant regions;~~

an SOI device gate on the thin gate oxide layer; and

the one or more additional gate regions being on the thicker gate oxide layer.

18. (Previously Presented): The SOI device as recited in claim 11, further comprising:

the thicker gate oxide layer being a selective epitaxy growth.

19. (Previously Presented): The SOI device as recited in claim 11, further comprising:

the substrate having an STI enclosure for the discrete implant regions.

20-35. (Cancelled)

36. (Currently Amended): An SOI device having a gate, comprising:

oxygen ions providing discrete implant regions in a substrate of an SOI device, the discrete implant regions extending to a surface of the substrate;

one or more additional gate regions forming an H-gate or a T-gate and covering the discrete implant regions, and,

a gate oxide layer formed over the surface and covering the discrete implant regions and being under the one or more additional gate regions, the gate oxide layer having ~~the same~~ a greater thickness over the discrete implant regions ~~and~~ than over regions other than the discrete implant regions,

the discrete implant regions forming gate oxide regions and reducing substrate resistance under each of the additional gate regions.

37. (Previously Presented): The SOI device of claim 11, further comprising doped ion implants under at least one of the one or more additional gate regions, the doped ion implants forming a source and drain in the substrate.

38. (Previously Presented): The SOI device of claim 37 wherein the substrate is a P-substrate, and the doped ion implants are N+ doped ions.

39. (Previously Presented): The SOI device of claim 37 wherein the substrate is an N-substrate, and the doped ion implants are P+ doped ions.

40. (Previously Presented): The SOI device of claim 36, further comprising doped ion implants under at least one of the one or more additional gate regions, the doped ion implants forming a source and drain in the substrate.

41. (Currently Amended): An SOI device having a gate, comprising:

a plurality of gate regions forming an H-gate or a T-gate and covering thick ~~first~~ oxide regions and thin ~~second~~ oxide regions,

each said thick ~~first~~ oxide region comprising a discrete implant region of oxygen ions formed in a substrate of an SOI device and extending to a surface of the substrate, and an oxide layer formed over but not encroaching the surface; and

each said thin ~~second~~ oxide region comprising only said oxide layer,

said oxide layer having substantially the same thickness in said thick ~~first~~ oxide regions and said thin ~~second~~ oxide regions.

42. (Previously Presented): The SOI device of claim 41, further comprising doped ion implants under at least one of the plurality of gate regions, the doped ion implants forming a source and drain in the substrate.

43. (Previously Presented): The SOI device of claim 42 wherein the substrate is a P-substrate, and the doped ion implants are N+ doped ions.

44. (Previously Presented): The SOI device of claim 42 wherein the substrate is an N-substrate, and the doped ion implants are P+ doped ions.

45. (Previously Presented): The SOI device of claim 42 wherein each of the plurality of gate regions is formed of polysilicon and includes sidewall spacers on opposed sidewalls thereof.

46. (Previously Presented): The SOI device of claim 41 wherein each of the plurality of gate regions is formed of polysilicon.

Allowable Subject Matter

Claims 11-12, 14-19, 36-46 are allowed.

The following is an examiner's statement of reasons for allowance: Prior art of record fails to teach nor suggest the combination of limitations found within claims 11, 36, and 41 as recited therein. The remaining claims are dependent and act only to further narrow the allowable subject matter and are therefore also allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Menz whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Laura M Menz/
Primary Examiner, Art Unit 2813

07/03/08